AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) An equalization circuit to receive a plurality of input symbols and to generate an output signal wherein the output signal is representative of a transmitted symbol, the equalization circuit comprising:

a first data slicer having a plurality of inputs and an output, wherein a first input is adapted to receive the plurality of input symbols and a second input is adapted to receive a first slicer level, and wherein the first data slicer outputs a first or second value based on the amplitude of the input symbol relative to the first slicer level;

a second data slicer having a plurality of inputs and an output, wherein a first input of the second data slicer is adapted to receive the plurality of input symbols and a second input of the second data slicer is adapted to receive a second slicer level, and wherein the second data slicer outputs the first or second value based on the amplitude of the input symbol relative to the second slicer level; and

logic circuitry, coupled to the first and second data slicers, to output a signal having either a first or second logic level wherein the first logic level is associated with the first value and the second logic level is associated with the second logic level, and wherein:

if the data slicers output the same value, the logic circuitry outputs the logic level that is associated with the value output by the data slicers; and

if the data slicers output different values, the logic circuitry outputs the complement of the logic level of the immediately preceding input symbol.~~; and~~

~~margining circuitry to measure the value of an error signal of a level sampling point~~

2. (Original) The equalization circuit of claim 1 wherein the first and second data slicers each include at least one voltage comparator.

3. (Original) The equalization circuit of claim 2 wherein the first and second data slicers each include a plurality of serially coupled sense amplifiers.

4. (Original) The equalization circuit of claim 1 further including adaptive circuitry, coupled to the first data slicer, to determine the first slicer level during operation of the equalization circuit and to provide the first slicer level to the first data slicer.

5. (Currently Amended) A receiver, coupled to a communications channel, to receive a plurality of input symbols transmitted by a transmitter, and to generate an output signal that is representative of each transmitted symbol, the receiver comprising:

equalization circuitry, coupled to the communications channel to receive the plurality of input symbols, the equalization circuitry including:

a first data slicer having a plurality of inputs and an output, wherein a first input is adapted to receive the plurality of input symbols and a second input is adapted to receive a first slicer level, and wherein the first data slicer outputs a first or second value based on the amplitude of the input symbol relative to the first slicer level;

a second data slicer having a plurality of inputs and an output, wherein a first input of the second data slicer is adapted to receive the plurality of input symbols and a second input of the second data slicer is adapted to receive a second slicer level, and wherein the second data slicer outputs the first or second value based on the amplitude of the input symbol relative to the second slicer level;

logic circuitry, coupled to the first and second data slicers, to output a signal having either a first or second logic level wherein the first logic level is associated with the first value and the second logic level is associated with the second logic level, and wherein:

if the data slicers output the same value, the logic circuitry outputs the logic level that is associated with the value output by the data slicers; and

if the data slicers output different values, the logic circuitry outputs the complement of the logic level of the immediately preceding input symbol; and

~~margining circuitry to measure the value of an error signal of a level sampling point; and~~

a memory, coupled to the second input of each data slicers, wherein the memory stores information which is representative of the first and second slicer levels.

6. (Original) The receiver of claim 5 further including adaptive circuitry, coupled to the second input of each data slicers, wherein the adaptive circuitry adjusts the first and second slicer levels in accordance with the performance of the receiver.

7. (Original) The receiver of claim 5 further including adaptive circuitry, coupled to the second input of the first data slicer, wherein the adaptive circuitry

changes the first data slicer level based on an upper edge and a lower edge of a receive eye of the first data slicer.

8. (Original) The receiver of claim 7 further including margining circuitry, coupled to the adaptive circuitry, wherein the margining circuitry determines the upper inner edge and the lower inner edge of the receive eye of the first data slicer.

9. (Original) The receiver of claim 8 wherein the margining circuitry includes a margining slicer having a plurality of inputs and an output, wherein a first input of the margining slicer is adapted to receive the plurality of input symbols and a second input is adapted to receive a margining slicer level, and wherein the margining slicer outputs a first or second value based on the amplitude of the input symbol relative to the margining slicer level.

10. (Original) The receiver of claim 9 wherein the margining circuitry includes reference level adjustment circuitry to generate the margining slicer level.

11. (Original) The receiver of claim 10 wherein the reference level adjustment circuitry generates margining slicer levels that vary according to the margining algorithm.

12. (Original) The receiver of claim 7 further including adaptive circuitry, coupled to the second input of the second slicer, wherein the adaptive circuitry changes the second slicer level based on an upper edge and a lower edge of a receive eye of the second slicer.

13. (Original) The receiver of claim 12 further including margining circuitry, coupled to the adaptive circuitry, wherein the margining circuitry determines the location of the upper inner edge and the lower inner edge of the receive eyes of the first and second slicer.

14. (Original) The receiver of claim 12 wherein the margining circuitry includes a margining slicer having a plurality of inputs and an output, wherein a first input of the margining slicer is adapted to receive the plurality of input symbols and a second input is adapted to receive a margining slicer level, and wherein the margining slicer outputs a first or second value based on the amplitude of the input symbol relative to the margining slicer level.

15. (Original) The receiver of claim 14 wherein the margining circuitry includes reference level adjustment circuitry to generate the margining slicer level.

16. (Original) The receiver of claim 15 wherein the reference level adjustment circuitry generates margining slicer levels that vary according to the margining algorithm.

17. (Currently Amended) The receiver of claim 15 further including:

a first ~~data~~ phase slicer having a plurality of inputs and an output, wherein a first input is adapted to receive the plurality of input symbols and a second input is adapted to receive a first slicer level, and wherein the first ~~data~~ phase slicer outputs a first or second value based on the amplitude of the input symbol relative to the first slicer level;

a second ~~data~~ phase slicer having a plurality of inputs and an output, wherein a first input of the second ~~data~~ phase slicer is adapted to receive the plurality of input symbols and a second input ~~of the second data slicer~~ is adapted

to receive a second slicer level, and wherein the second ~~data~~ phase slicer outputs the first or second value based on the amplitude of the input symbol relative to the second slicer level;

margining circuitry to measure the value of an error signal of a ~~level~~ phase sampling point; and

adaptive circuitry, coupled to margining circuitry and the second input of the first slicer, wherein the adaptive circuitry changes the first slicer level based on the value of the error signal.

18. (Original) The receiver of claim 17 wherein the margining circuitry includes a margining slicer having a plurality of inputs and an output, wherein a first input of the margining slicer is adapted to receive the plurality of input symbols and a second input is adapted to receive a margining slicer level, and wherein the margining slicer outputs a first or second value based on the amplitude of the input symbol relative to the margining slicer level.

19. (Currently Amended) A receiver, coupled to a communications channel, to receive a plurality of input symbols transmitted by a transmitter, and to generate an output signal that is representative of each transmitted symbol, the receiver comprising:

equalization circuitry, coupled to the communications channel to receive the plurality of input symbols, the equalization circuitry including:

a first data slicer having a plurality of inputs and an output, wherein a first input is adapted to receive the plurality of input symbols and a second input is adapted to receive a first slicer level, and wherein the first data slicer outputs a first or second value based on the amplitude of the input symbol relative to the first slicer level;

a second data slicer having a plurality of inputs and an output, wherein a first input of the second data slicer is adapted to receive the plurality of input

symbols and a second input of the second data slicer is adapted to receive a second slicer level, and wherein the second data slicer outputs the first or second value based on the amplitude of the input symbol relative to the second slicer level;

logic circuitry, coupled to the first and second data slicers, to output a signal having either a first or second logic level wherein the first logic level is associated with the first value and the second logic level is associated with the second logic level, and wherein:

if the data slicers output the same value, the logic circuitry outputs the logic level that is associated with the value output by the data slicers; and

if the data slicers output different values, the logic circuitry outputs the complement of the logic level of the immediately preceding input symbol;

margining circuitry, including at least one margining slicer, to determine at least one performance parameter of the receiver~~the value of an error signal of a level sampling point~~; and

adaptive circuitry, coupled to the margining circuitry and the second input of the first data slicer, wherein the adaptive circuitry adjusts the first slicer level based on the at least one performance parameter.

20. (Original) The receiver of claim 19 wherein the at least one performance parameter of the receiver includes an upper inner edge and a lower inner edge of a receive eye of the first data slicer.

21. (Original) The receiver of claim 19 wherein the at least one performance parameter of the receiver includes an upper edge and a lower edge of a receive eye of the second data slicer.

22. (Original) The receiver of claim 19 wherein the at least one performance parameter of the receiver includes error signal of a phase sampling point.

23. (Original) The receiver of claim 19 wherein the margining slicer includes a plurality of inputs and an output, wherein a first input of the margining slicer is adapted to receive the plurality of input symbols and a second input is adapted to receive a margining slicer level, and wherein the margining slicer outputs a first or second value based on the amplitude of the input symbol relative to the margining slicer level.

24. (Original) The receiver of claim 23 wherein the margining circuitry includes reference level adjustment circuitry to generate the margining slicer level.

25. (Original) The receiver of claim 24 wherein the reference level adjustment circuitry generates margining slicer levels that vary according to the margining algorithm.

26. (Original) The receiver of claim 19 wherein the first, second and margining data slicers each include a plurality of serially coupled sense amplifiers.